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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	Not assigned yet
				Filing Date	On even date herewith
				First Named Inventor	K. OSADA, et al.
				Art Unit	Not assigned yet
				Examiner Name	Not assigned yet
Sheet	1	of	1	Attorney Docket Number	500.35578CC5

U.S. PATENT DOCUMENTS						
Examiner Initials ¹	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
HAR		5,253,207		10/93	Shikataki	
		5,675,529		10/97	Poola	
		5,574,687		11/96	Nakase	
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FOREIGN PATENT DOCUMENTS							
Examiner Initials ¹	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ² -Number ⁴ -Kind Code ⁵ (if known)					
HAR ↑ HAR		4-85788		3/18/92			
		3-216882		8/24/81			
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		2-50396		2/90			
		7-201187		8/95			

OTHER PRIOR ART—NON PATENT LITERATURE DOCUMENTS			
Examiner Initials ¹	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
HAR		Osada et al., "A 2ns Access, 285MHz, Two-Port Cache Macro Using Double Global Bit-Line Pairs" ISSCC Digest of Technical Papers, pp. 402-403	
HAR		Kushiyami et al., "A 295MHz CMOS 1M (x256) Embedded SRAM Using Bi-directional Read/Write Shared Sense Amps and Self-Timed Pulsed Word-Line Drivers" ISSCC Digest of Technical Papers, Feb. 1995, pp. 304-305	
HAR		IEEE Journal of Solid State Circuits, Vol. 23, No. 5, Oct. 1988, pp. 1048-1053	

Examiner Signature	H. H.	Date Considered	3/16/04
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